Hardware/Software Codesign Midterm 2 Lab Test

In this test, you are required to create a custom IP, named my\_gpio\_ip, and add it to IP Repository. You will be provided with the source code of this IP in Verilog. Then based on Lab 2, add an instant of this new ip, use this new IP instant to control the onboard LEDs. You are required to use user defined register 2 to control the LEDs. The behavior of the LEDs is the same as Lab 4: use the 4 onboard dip switch to turn on/off the corresponding LEDs. Your application project folder will be named using the following format: midterm2\_your first name, your IP project folder will be named my\_gpio\_ip.

You will start from Lab 2, rename it to midterm2\_your first name, and then start your application project from this renamed project.

You will also be provided with the following files:

1. my\_gpio\_ip\_user\_logic.v: Verilog source code for the custom IP to be added
2. user\_logic\_instantiation: code for instantiating new\_led\_ip\_user\_logic
3. my\_gpio\_ip\_user\_constrain.xdc: the user constrain files needed for LEDs
4. midterm2.c: Start up C code for your application project

You are also free to use any one of the five lab manuals we used in this course to figure out steps and operations needed.

**Extra challenge (5 points)**: modify my\_gpio\_ip.v and my\_gpio\_ip\_user\_logic.v to take care of both input and output devices. Use my\_gpio\_ip to control the onboard push button. Add the following feature to your embedded system: when a push button is pressed, the corresponding led will flash; release the push button will stop the flash.

When you are done with your test, demonstrate your project on board, submit a copy of your project to Beachboard dropbox (folders midterm2\_your first name and new\_led\_ip in zip file) and then submit the following items in one Word document.

1. Software source code: midterm2.c
2. Hardware source code: new\_led\_ip\_user\_logic.v
3. Answer the following questions:
4. Specify the location(s) for the DDR3 Controller and DDR3 memory: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.
5. Specify the location(s) for the new\_led\_ip instance: inside [Xilinx Zynq-7000 (XC7Z010-1CLG400C)](http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/silicon-devices.html) or outside? If inside, specify if it is a hard core or soft cores and where does it locate in XC7Z010-1CLG400C: in PS or PL.
6. List all the external peripherals in the embedded system you build in this project.